In the Claims:

1. (Previously presented) A method of manufacturing on a substrate a 2-transistor memory cell comprising a storage transistor having a memory gate stack and a selecting transistor, there being a tunnel dielectric layer between the substrate and the memory gate stack, the method comprising:

forming the memory gate stack by

providing a first conductive layer on the tunnel dielectric layer and a second conductive layer with a deposited interlayer dielectric layer between the first and second conductive layers, the deposited interlayer dielectric layer including oxide and being susceptible to undesirable growth upon exposure to oxygen during subsequent oxidation steps,

etching the second conductive layer thus forming a control gate,

forming spacers against the control gate in the direction of a channel to be formed under the tunnel dielectric layer, the spacers being formed from a dielectric material having an oxygen diffusion through the dielectric material that is, relative to oxide spacers, an order of magnitude smaller than oxygen diffusion through the oxide spacers, and

thereafter using the spacers as a hard mask to etch the first conductive layer thus forming the floating gate, the etching of the first conductive layer being an anisotropic dry etch that is selective to the tunnel dielectric, thereby using the tunnel dielectric to protect portions of the substrate laterally adjacent to the floating gate;

removing a portion of the tunnel dielectric laterally adjacent to the floating gate and exposing a portion of the substrate where the tunnel dielectric has been removed; and

forming an access gate dielectric oxide on the exposed portion of the substrate, using the spacers to mitigate the diffusion of oxygen to the deposited interlayer dielectric layer.

2. (Cancelled).

3. (Previously presented) A method according to claim 1, wherein the dielectric material having an oxygen diffusion through the material that is an order of magnitude smaller

than oxygen diffusion through oxide spacers includes one or more of silicon nitride, silicon carbide or metal oxide.

4. (Previously presented) A method according to claim 1, furthermore comprising,

before forming the memory gate stack, applying the tunnel dielectric layer on the substrate, and

after formation of the memory gate stack, removing the tunnel dielectric layer by a selective etching technique at least at a location where the selecting transistor is to be formed, the selective etching technique preferentially etching the tunnel dielectric layer compared to the substrate.

5. (Previously presented) A method according to claim 1, further including forming

a floating gate dielectric next to the formed floating gate while forming the access gate dielectric.

6. (Previously presented) A method according to claim 1, furthermore comprising

removing part of the interlayer dielectric layer after forming the control gate but before forming the spacers.

7. (Previously presented) A method according to claim 1 wherein

forming an access gate includes forming the access gate while the spacer at the access gate side is still present.

8. (Withdrawn) A 2-transistor memory cell comprising,

a storage transistor and

a selecting transistor, the storage transistor comprising

a dielectric layer on a substrate,

a floating gate on the dielectric layer,

a deposited interlayer dielectric layer on the floating gate,

a control gate on the interlayer dielectric layer and being smaller than the floating gate, and

spacers next to the control gate and made from a dielectric material having an oxygen diffusion through the dielectric material that is an order of magnitude smaller than oxygen diffusion through oxide spacers and that mitigates oxygen diffusion to the interlayer dielectric layer.

9. (Cancelled).

10. (Withdrawn) A memory cell according to claim 8, the selecting transistor comprising an access gate on an access gate dielectric on the substrate immediately adjacent to a wet-etched portion of the dielectric layer, one of the spacers being present between the control gate and the access gate, and a floating gate sidewall dielectric that is contiguous with the access gate dielectric and present between the floating gate and the access gate, wherein the one spacer is thicker than the floating gate sidewall dielectric.

11. (Withdrawn) An electronic device comprising a 2-transistor memory cell including,

a storage transistor and

a selecting transistor, the storage transistor comprising

a dielectric layer on a substrate,

a floating gate on the dielectric layer,

a deposited interlayer dielectric layer on the floating gate,

a control gate on the interlayer dielectric layer and being smaller than the floating gate, and

spacers next to the control gate and made from a dielectric material having an oxygen diffusion through the dielectric material that, relative to oxide spacers, is an order of magnitude smaller than the oxygen diffusion through the oxide spacers and that mitigates oxygen diffusion to the interlayer dielectric layer.

12. (Cancelled).

13. (Withdrawn) The electronic device as recited in claim 11, wherein the selecting transistor includes,

an access gate on an access gate dielectric on the substrate immediately adjacent to a wet-etched portion of the dielectric layer one of the spacers being present between the control gate and the access gate, and

a floating gate sidewall dielectric that is contiguous with the access gate dielectric and present between the floating gate and the access gate, wherein the one spacer is thicker than the floating gate sidewall dielectric.

14. (Previously presented) A method according to claim 1,

wherein removing a portion of the tunnel dielectric includes wet etching the tunnel dielectric to remove a portion of the tunnel dielectric laterally adjacent to the floating gate and expose a portion of the substrate surface where the tunnel dielectric has been wet etched, leaving the exposed surface of the substrate intact, and

further including forming an access gate of the selecting transistor on the access gate dielectric.

15. (Withdrawn) The memory cell of claim 10, further comprising:

a cap layer on the control gate, the one spacer being located between the cap layer and the access gate and the one spacer being in contact with the cap layer, the control gate, the access gate and the floating gate;

another floating gate sidewall dielectric located on a sidewall of the floating gate opposite from the floating gate sidewall dielectric; and

offset spacers, one of the offset spacers being in contact with the access gate, and another one of the offset spacers being in contact with the other floating gate sidewall dielectric and in contact with another one of the spacers that is located on a side of the control gate opposite from the one spacer.

16. (Withdrawn) The electronic device of claim 13, further comprising:

a cap layer on the control gate, the one spacer being located between the cap layer and the access gate and the one spacer being in contact with the cap layer, the control gate, the access gate and the floating gate;

another floating gate sidewall dielectric located on a sidewall of the floating gate opposite from the floating gate sidewall dielectric; and

offset spacers, one of the offset spacers being in contact with the access gate, and another one of the offset spacers being in contact with the other floating gate sidewall dielectric and in contact with another one of the spacers that is located on a side of the control gate opposite from the one spacer.

17. (Currently Amended) A method of manufacturing a two-transistor memory cell comprising a storage transistor having a memory gate stack and a selecting transistor, the method comprising:

forming a tunnel dielectric on a substrate;

forming a first conductive layer on the tunnel dielectric ~~layer~~;

depositing an interlayer dielectric layer on the first conductive layer, the deposited interlayer dielectric layer including oxide and being susceptible to undesirable growth upon exposure to oxygen during subsequent oxidation steps;

forming a second conductive layer on the interlayer dielectric layer;

etching the second conductive layer to form a control gate;

forming a selecting transistor on the substrate laterally adjacent to the first conductive layer and having an access gate on an access gate dielectric;

forming spacers against sides of the control gate, the spacers being formed from a dielectric material having an oxygen diffusion through the dielectric material that is, relative to oxide spacers, an order of magnitude smaller than oxygen diffusion through the oxide spacers, one of the spacers being formed between the control gate and the access gate;

using the spacers to mask underlying portions of the interlayer dielectric layer and the first conductive layer, etching the first conductive layer to form a floating gate using an anisotropic dry etch that is selective to the tunnel dielectric, using the tunnel dielectric to mask portions of the substrate laterally adjacent to the floating gate;

forming a floating gate sidewall dielectric that is contiguous with the access gate dielectric and present between the floating gate and the access gate, wherein the one of

the spacers being formed between the control gate and the access gate is thicker than the floating gate sidewall dielectric;

removing a portion of the tunnel dielectric laterally adjacent to the floating gate and exposing a portion of the substrate where the tunnel dielectric has been removed; and

forming an access gate dielectric oxide on the exposed portion of the substrate, using the spacers to mitigate the diffusion of oxygen to the deposited interlayer dielectric layer.

18. (Previously presented) The method of claim 17, further comprising forming a cap layer on the second conductive layer,

wherein forming spacers includes forming the one spacer, which is formed between the control gate and the access gate, between the cap layer and the access gate and in contact with the cap layer, the control gate, the access gate and the floating gate.

19. (Previously presented) The method of claim 17, further comprising forming a cap layer on the second conductive layer,

wherein forming spacers includes forming the one spacer, which is formed between the control gate and the access gate, between the cap layer and the access gate and in contact with the cap layer, the control gate, the access gate and the floating gate,

further including forming another floating gate sidewall dielectric located on a sidewall of the floating gate opposite from the floating gate sidewall dielectric, and

further including forming offset spacers, one of the offset spacers being in contact with the access gate, and another one of the offset spacers being in contact with the other floating gate sidewall dielectric and in contact with another one of the spacers that is located on a side of the control gate opposite from the one spacer.